74HC138; 74HCT138

3-to-8 line decoder/demultiplexer; inverting

Product data sheet

1. General description

The 74HC138; 74HCT138 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC138; 74HCT138 decoder accepts three binary weighted address inputs (A0, A1 and A3) and when enabled, provides 8 mutually exclusive active LOW outputs ($\overline{Y}0$ to $\overline{Y}7$).

The 74HC138; 74HCT138 features three enable inputs: two active LOW ($\overline{E}1$ and $\overline{E}2$) and one active HIGH (E3). Every output will be HIGH unless $\overline{E}1$ and $\overline{E}2$ are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the 74HC138; 74HCT138 to a 1-of-32 (5 lines to 32 lines) decoder with just four 74HC138; 74HCT138 ICs and one inverter.

The 74HC138; 74HCT138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Not used enable inputs must be permanently tied to their appropriate active HIGH- or LOW-state.

The 74HC138; 74HCT138 is identical to the 74HC238; 74HCT238 but has inverting outputs.

2. Features

- Demultiplexing capability
- Multiple input enable for easy expansion
- Complies with JEDEC standard no. 7A
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

PHILIPS

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
74HC138							
t_{PHL}, t_{PLH}	propagation delay	V_{CC} = 5 V; C_L = 15 pF					
	An to $\overline{Y}$n			-	12	-	ns
	E3 to $\overline{Y}$n			-	14	-	ns
	$\overline{E}$n to $\overline{Y}$n			-	14	-	ns
C_i	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[1]	-	67	-	pF
74HCT138							
t_{PHL}, t_{PLH}	propagation delay	V_{CC} = 5 V; C_L = 15 pF					
	An to $\overline{Y}$n			-	17	-	ns
	E3 to $\overline{Y}$n			-	19	-	ns
	$\overline{E}$n to $\overline{Y}$n			-	19	-	ns
C_i	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance	V_I = GND to (V_{CC} − 1.5 V)	[1]	-	67	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC138				
74HC138N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HC138D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC138DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC138PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC138BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

Table 2: Ordering information *…continued*

Type number	Package			
	Temperature range	Name	Description	Version
74HCT138				
74HCT138N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74 HCT138D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT138DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT138PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT138BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

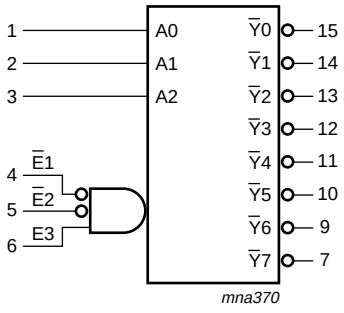


Fig 1. Logic symbol

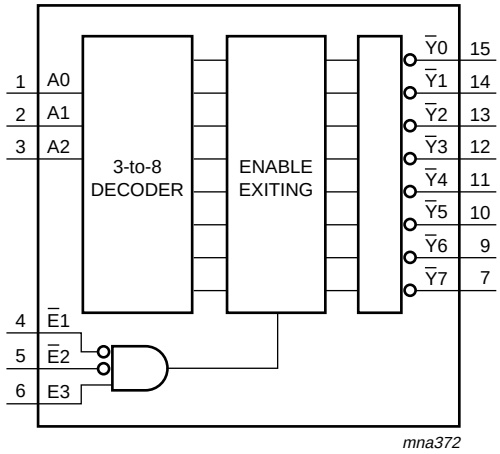


Fig 2. Functional diagram

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±20	mA
I_O	output current	$V_O = –0.5$ V to ($V_{CC} + 0.5$ V)		-	±25	mA
I_{CC}	quiescent supply current			-	50	mA
I_{GND}	ground current			-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation					
	DIP16 package		[1]	-	750	mW
	SO16 package		[2]	-	500	mW
	SSOP16 package		[3]	-	500	mW
	TSSOP16 package		[3]	-	500	mW
	DHVQFN16 package		[4]	-	500	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC138						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r, t_f	input rise and fall time	$V_{CC} = 2.0$ V	-	-	1000	ns
		$V_{CC} = 4.5$ V	-	6.0	500	ns
		$V_{CC} = 6.0$ V	-	-	400	ns
74HCT138						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r, t_f	input rise and fall time	$V_{CC} = 4.5$ V	-	6.0	500	ns

Table 8: Static characteristics 74HCT138

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 4.5 V	-	0.0	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V; $V_O = V_{CC}$ or GND; I_O = 0 A	-	-	±0.5	µA
I_{CC}	quiescent supply current	V_{CC} = 6.0 V; I_O = 0 A; $V_I = V_{CC}$ or GND	-	-	8.0	µA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
	pin An		-	150	540	µA
	pin $\overline{En}$		-	125	450	µA
	pin E3		-	100	360	µA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.84	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V; $V_O = V_{CC}$ or GND; I_O = 0 A	-	-	±5.0	µA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; I_O = 0 A; $V_I = V_{CC}$ or GND	-	-	80	µA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
	pin An		-	-	675	µA
	pin $\overline{En}$		-	-	562.5	µA
	pin E3		-	-	450	µA

Table 8: Static characteristics 74HCT138 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	3.7	-	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	1.0	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_{CC} = 5.5 V; V_O = V_{CC} or GND; I_O = 0 A	-	-	±10.0	µA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; I_O = 0 A; V_I = V_{CC} or GND	-	-	160	µA
ΔI_{CC}	additional quiescent supply current	per input pin; V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
	pin An		-	-	735	µA
	pin $\overline{E}$n		-	-	612.5	µA
	pin E3		-	-	490	µA

Table 10: Dynamic characteristics 74HCT138

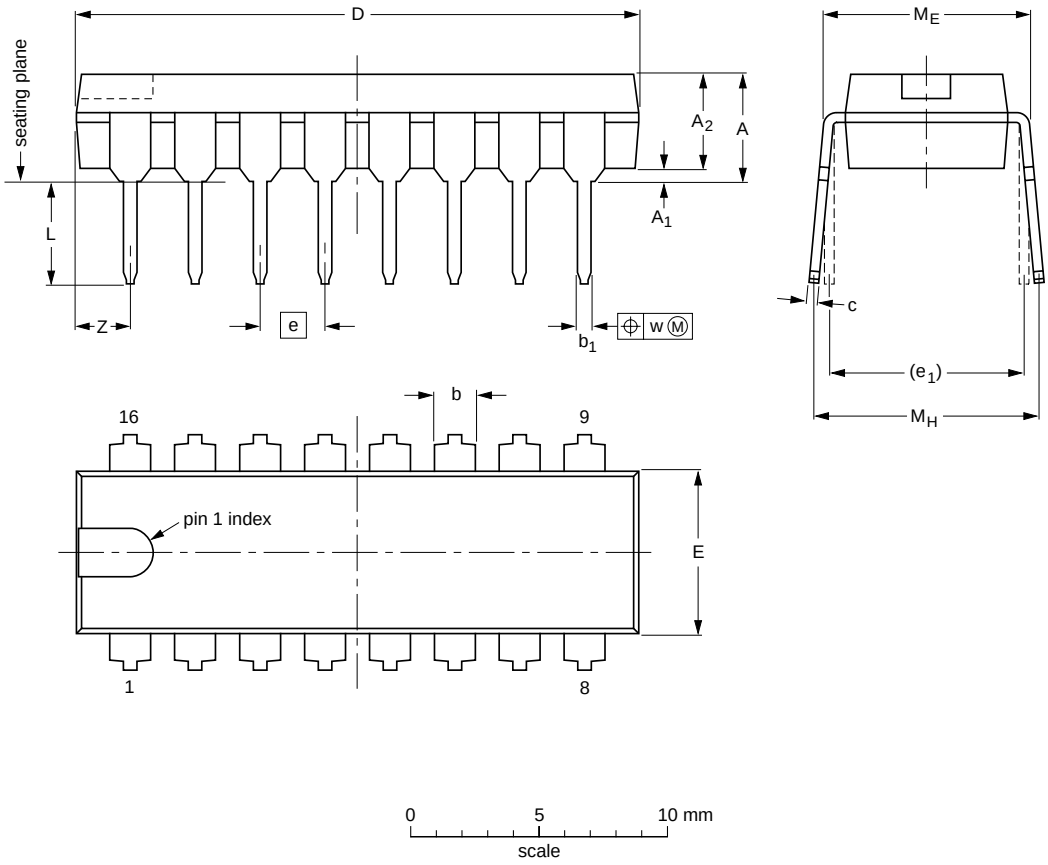
Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified. For test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PHL}, t_{PLH}	propagation delay					
	An to $\overline{Y}$n	see Figure 6				
		V_{CC} = 4.5 V	-	20	35	ns
		V_{CC} = 5 V; C_L = 15 pF	-	17	-	ns
	E3 to $\overline{Y}$n	see Figure 6				
		V_{CC} = 4.5 V	-	18	40	ns
		V_{CC} = 5 V; C_L = 15 pF	-	19	-	ns
	$\overline{E}$n to $\overline{Y}$n	see Figure 7				
		V_{CC} = 4.5 V	-	19	40	ns
		V_{CC} = 5 V; C_L = 15 pF	-	19	-	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6 and 7				
		V_{CC} = 4.5 V	-	7	15	ns
C_{PD}	power dissipation capacitance	V_I = GND to (V_{CC} – 1.5 V) [1]	-	67	-	pF
T_{amb} = –40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay					
	An to $\overline{Y}$n	see Figure 6				
		V_{CC} = 4.5 V	-	-	44	ns
	E3 to $\overline{Y}$n	see Figure 6				
		V_{CC} = 4.5 V	-	-	50	ns
	$\overline{E}$n to $\overline{Y}$n	see Figure 7				
		V_{CC} = 4.5 V	-	-	50	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6 and 7				
		V_{CC} = 4.5 V	-	-	19	ns
T_{amb} = –40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay					
	An to $\overline{Y}$n	see Figure 6				
		V_{CC} = 4.5 V	-	-	53	ns
	E3 to $\overline{Y}$n	see Figure 6				
		V_{CC} = 4.5 V	-	-	60	ns
	$\overline{E}$n to $\overline{Y}$n	see Figure 7				
		V_{CC} = 4.5 V	-	-	60	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6 and 7				
		V_{CC} = 4.5 V	-	-	22	ns

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

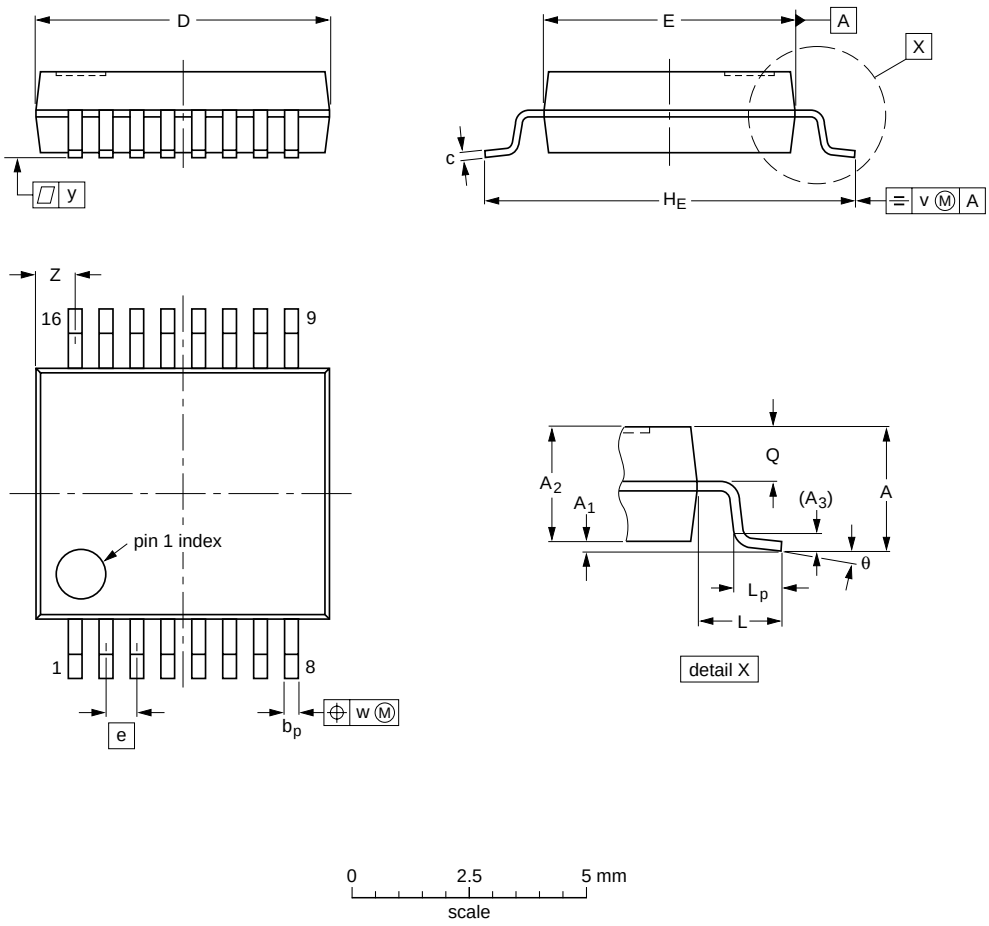
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			

Fig 9. Package outline SOT38-1 (DIP16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				

Fig 12. Package outline SOT338-1 (SSOP16)